LEVEL II

CALIFORNIA INSTITUTE OF TECHNOLOGY

PASADENA, CALIFORNIA 91125

COMPUTER SCIENCE 256-80

R&D STATUS REPORT

ARPA ORDER NO. 3771 Amend. No. 1

CONTRACTOR: Caltech

CONTRACT NUMBER: N00014-79-C-0924, NARPA Order-3771

EFFECTIVE DATE OF CONTRACT: September 1, 1979

EXPIRATION DATE OF CONTRACT: October 15, 1980

1 Sep 80

PRINCIPAL INVESTIGATOR: Carver/Mead

TELEPHONE NUMBER: (213) 356-6811

SHORT TITLE: Demonstration of the Use of VLSI Design Rules, Standards, and Interfaces.

REPORTING PERIOD: June 1, 1980 to September 1, 1980

Research and development status rept. 1 Jun-1 Sep 80

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CALIFORNIA INSTITUTE OF TECHNOLOGY

PASADENA, CALIFORNIA 91125

COMPUTER SCIENCE 256-80

3 June 1981

Col. Duane Adams
Advanced Research Projects Agency
1400 Wilson Boulevard
Arlington, Virginia 22209

Dear Sir:

Enclosed please find copies of interim technical reports for the periods: June 1, 1980 through September 1, 1980; September 1, 1980 through December 1, 1980; and December 1, 1980 through March 1, 1981; for Contract No. N00014-79-C-0924, "Demonstration of the Use of VLSI Design Rules, Standards, and Interfaces", ARPA Order No. 3771, Amendment No. 1.

Sincerely,

Carver A. Mead
Gordon & Betty Moore Professor
of Computer Science

CAM:pw:#4518
Enc.

cc: Director, NRL, Washington
Defense Documentation Center, Washington
Mr. Clint Werner, ONR, Pasadena
Dr. Clifford Lau, ONR, Pasadena
Dr. Elliott Cohen, ONR, Washington
Mr. A. J. Lindstrom, CIT

DESCRIPTION OF PROGRESS

Progress is reported for each element of Tasks 1 and 2.

TASK 1

1. Consultation from Fabrication Lines

Technical inputs from the industrial fabricators (consultants) were completed by telephone discussions and visits by T. W. Griswold. A written report has been received from Hughes. The Rockwell and Honeywell reports are expected in early September. The CMOS-SOS design rules were accepted with the exception that island polysilicon butting contacts were not endorsed by any of the fabrication houses. As a result, an alternate contact structure was defined. The test-chip was accepted with suggestions for some minor modifications and additional experimental structures.

2. CMOS-SOS and NMOS-Si Gate Test-Chips

The NMOS test-chip designs were fabricated as a part of MPC580. Chips have been received at JPL and limited testing has been done. As a result of testing and further evaluation, changes in the test-chip were made. These include:

1. Removal of the common sharing of probe pads.

2. Addition of more contact resistors.

3. Additional transistors with varying width to length ratios.

JPL had discussions with NBS, HP, and Xerox on foundry test-chip makeup and standard foundry test-structure layout. It was decided that these would be implemented by JPL using the standard NBS probe-pad array.

These revisions were incorporated in the NMOS test-chip design. The new design was submitted for fabrication as part of MPC880.

Design of the JPL CMOS-SOS test-chip was started.

A test-chip workshop was held at Caltech on August 20, 1980. The workshop was well attended by people throughout industry and the government (a list of attendees is attached). The workshop allowed people to discuss their particular test-chip activity and to express their views. JPL presented the test-chip and test-strip for NMOS foundry runs. The group was supportive of what was presented.

3. Geometrical Design Rules

IIL design rules were received from Boeing. The rules were very similar to those used for NMOS. This similarity encourages our feeling that a general approach to GDR definition can be developed that will be applied to several technologies.

A consultant was not found to generate a set of CMOS-bulk design rules. This task has been deferred since it is not a formal part of the program.

As stated above, the CMOS-SOS GDR's have been created and accepted by the fabricators.

4. Speed and Timing Rules

A draft version of the final report for speed and timing rules has been received. The report has been reviewed by JPL and Caltech personnel and returned to Fred Rosenberger for modifications prior to inclusion in the overall final report. Suggestions for changes included:

1. Writing a short version for direct inclusion in the final report; the full version will be issued separately as a reference document.

2. Highlighting those rules that address the speed and timing problems arising from decreasing feature size.

5. CIF

Work complete; no further progress.

6. Testability Rules

The development of criteria and rational for testability is proceeding under the direction of Chuck Sietz at Caltech and in collaboration with graduate student Erik DeBenedictis. The final results for this task will be derived, in part, from work being done at Caltech under the Submicron Systems Architecture contract, ARPA No. 3771, ONR contract No. N00014-79-C-0597. Therefore, no direct charges have been made to this program, nor is it anticipated that they will. The criteria and rational will be derived from the work previously mentioned.

TASK 2

1. Design-Rule Checker

Deleted (see last quarterly report).

2. CIF/APPLICON, CALMA Conversion Software

During this reporting period, approximately 50% of the software development for CIF to APPLICON was achieved. It has been decided that only the software for converting CIF to APPLICON would be developed. Conversion to other formats, such as MEBES or CALMA, can be obtained directly from APPLICON.

3. Circuit Design

The memory interface building block design in NMOS was fabricated as part of MPC580. Chips were received and tested. The results of the tests have shown a minor design error which caused the circuit to be inoperative. The design error was corrected and the circuit was resubmitted to be fabricated as part of MPC880.

The memory interface building block was also designed using MP2D. It was orginally intended that MP2D software would be available for use on JPL/Caltech computers. Some difficulties were encountered, however, and it was decided to use the Army facilities at Ft. Mommouth, N.J. instead. The MP2D design exists in software but there are no plans for fabrication.

Conclusions reached regarding the MP2D design were that it was easier to design (approximately two weeks) but took up slightly more area (up to 20%). One compromise that had to be made was the degree that self checking could be included. Because of the nature of the standard cells that were available, it was not possible to make the design 100% self checking.

CHANGES IN KEY PERSONNEL: none

SUMMARY OF SUBSTANTIVE INFORMATION DERIVED FROM SPECIAL EVENTS: none

PROBLEMS ENCOUNTERED OR ANTICIPATED: none

ACTION REQUIRED BY THE GOVERNMENT: none

FISCAL STATUS:

1. Amount currently on contract: $457,080

2. Expenditures and commitments to date:

Campus Salaries and Contracts:	4,615	
JPL Salaries and Contracts:	383,680	
		$388,295

3. Funds required to complete Tasks 1 and 2: $68,785

Note: the "Campus Salaries and Contracts" item for last reporting period was inccorrectly shown as $9,066. The correct value was $4,539.

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